High performance ZnO nanowire field effect transistor using self-aligned nanogap gate electrodes

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A field effect transistor (FET) using a zinc oxide nanowire with significantly enhanced performance is demonstrated. The device consists of single nanowire and self-aligned gate electrodes with well defined nanosize gaps separating them from the suspended nanowire. The fabricated FET exhibits excellent performance with a transconductance of 3.06 μS, a field effect mobility of 928 cm^2/V s, and an on/off current ratio of 10^6. The electrical characteristics are the best obtained to date for a ZnO transistor. The FET has a *n*-type channel and operates in enhancement mode. The results are close to those reported previously for *p*-type carbon nanotube (CNT) FETs. This raises the possibility of using ZnO as the *n*-type FET with a CNT as the *p*-type FET in nanoscale complementary logic circuits. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2416249]

One-dimensional nanostructures such as carbon nanotubes (CNTs),[1] gallium nitride nanowires,[2] and zinc oxide (ZnO) nanowires[3] are anticipated to provide functional building blocks for future nanoscale electronic, optical, optoelectronic, electrochemical, and electromechanical systems.[4–6] The ZnO nanowire is a II-VI semiconductor with a direct band gap (E_g=3.37 eV at 300 K) and a relatively large exciton binding energy ($\sim$60 meV). Its potential as a gas sensor, optical sensor, and transistor has been explored previously.[7–11] Transistor studies to date have shown limited performance without doping or chemical treatments of the nanowire.[10,11]

In this letter, we report a high performance ZnO nanowire FET, which has a self-aligned gate and nanosize air gap capacitors. The nanowire is suspended between the source and drain electrodes. Leakage current through gate and channel, which is more prevalent in a solid insulator, can be avoided by using nanosize air gaps. The nanowires were prepared by the vapor-liquid-solid mechanism[12] and have typical lengths of 3.0–10.0 μm and diameters of 30–100 nm. They were produced with a 1:1 ZnO:C ratio at 950 °C on a gold coated silicon substrate. Four point probe measurements under dark condition give a typical resistivity of $\sim$7.5 Ω cm. Niobium (Nb) was chosen for the source and the drain electrodes because its work function (4.30 eV) is well matched to the electron affinity of the ZnO channel (4.35 eV).[13] The nanowires show Ohmic transport properties with Nb contacts at room temperature in an air ambient. The substrate used for device fabrication was *n*-type silicon (Si) with 1000 nm of deposited SiO_2. An 80 nm aluminum (Al) layer was deposited on the substrate to act as a sacrificial layer. The thickness of the Al layer determines the suspension height of the nanowire above the substrate. Initially ZnO nanowires dispersed in isopropyl alcohol were spin coated on the substrate. After mapping the ZnO nanowires by imaging in a scanning electron microscope (SEM S800 Hitachi, 20 kV), the nanowire contact electrodes (source and drain electrodes) were formed on both ends of the nanowires by electron beam lithography and sputtering of 200 nm of Nb. Following Al sacrificial layer removal, a second electron beam lithography step was carried out for fabrication of the self-aligned in plane gate electrodes[14] oriented normal to the nanowire on either side. Chromium (Cr) was evaporated on the patterned electron beam resist, poly(methylmethacrylate) (PMMA), followed by a lift-off process to form the electrodes. The gate electrodes are separated by the ZnO nanowires acting as an evaporation mask when the metal film is deposited into the patterned PMMA region forming the gate. Lift-off of the metal (Cr) on the ZnO nanowire is readily achieved due to its poor adhesion to the ZnO nanowires and poor step coverage of the evaporated metal. The SEM image in Fig. 1 shows the metal-air gap-semiconductor field effect transistor (MASFET) consisting of a single ZnO nanowire and two self-aligned electrodes (gate electrodes). Each dimension of the ZnO nanowire FET such as channel length (968 nm), thick-

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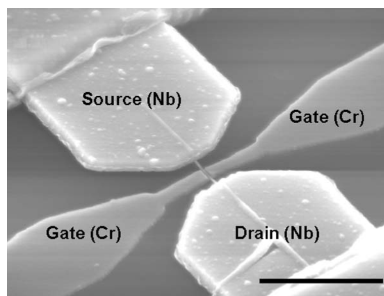

FIG. 1. 45° tilted SEM image of fabricated ZnO nanowire FET with self-aligned gate electrodes and nanosize air gaps. Scale bar is 2.5 μm.

ness of gate insulator (air gap, 26 nm), channel width (diameter of the nanowire, 60 nm), and gate width (360 nm) was measured on completion of the entire fabrication process.

Electrical measurements were performed with a probe stage in an ambient environment (at room temperature in air and dark conditions). An HP 4150A picoammeter and voltage-current source were used under computer control. Figure 2(a) shows the drain current versus drain voltage (I_{ds}-V_{ds}) output characteristics as a function of gate voltage. The drain current versus gate voltage (I_{ds}-V_{gs}) transfer characteristic at a V_{ds} of 0.8 V is shown in Fig. 2(b). The I_{ds}-V_{ds} curves indicate that the MASFET operates in n-channel enhancement mode. The gate transfer characteristic shows an on/off current ratio of 10^6 with a very low off current level ($\sim 10^{-12}$ A), a subthreshold slope of 129 mV/decade, and a threshold voltage (V_{th}) of 0.4 V. The transconductance (g_m) is 3.06 μS [insert of Fig. 2(b)] and the normalized transconductance (g_m/channel width) is 51.2 μS/μm, which is smaller but comparable with those from CNTs [generally quoted in units of transconductance per unit width (μS/μm)]. Since the diameter, equivalent to a channel width in a conventional transistor, of a single wall carbon nanotube (SWCNT) is of the order of 1.5–3 nm compared to 60 nm in the case of the ZnO nanowire, it appears that a CNT has a per unit transconductance which is 5–20 times higher, although the measured total current is similar to that in the ZnO FET. However, it is difficult to scale a CNT transistor for a desired current by simply expanding the width of the transistor, which is what is implied by using the normalized transconductance as a measure of performance. Technology to scale transistor current by paralleling more than one SWCNT in a controlled way (i.e., having the same semiconducting properties) is not available at present. Bundle transistors are not controlled and have a mixture of metallic and semiconducting CNTs. This means in practice it is still to be shown that within a 60 nm width, significantly higher than 3–5 μA can be obtained from a CNT transistor,[15–17] which is the same as measured for the ZnO MASFET. ZnO transistor output characteristic in Fig. 2(a) reveals an output conductance of 1.47 μS at a gate voltage of 0.8 V (with V_{ds} in the range of 0.25–1.5 V). Comparing this with the transconductance characteristic shown in the insert of Fig. 2(b), it is clearly seen that the ZnO MASFET has a gain >2 (transconductance/output conductance) over a practical range of input and output voltages. This is a very important achievement in that it verifies that the ZnO MASFET can be used as a transistor in circuits. The gain of the MASFET can be enhanced further through optimization of the gate width and channel length.

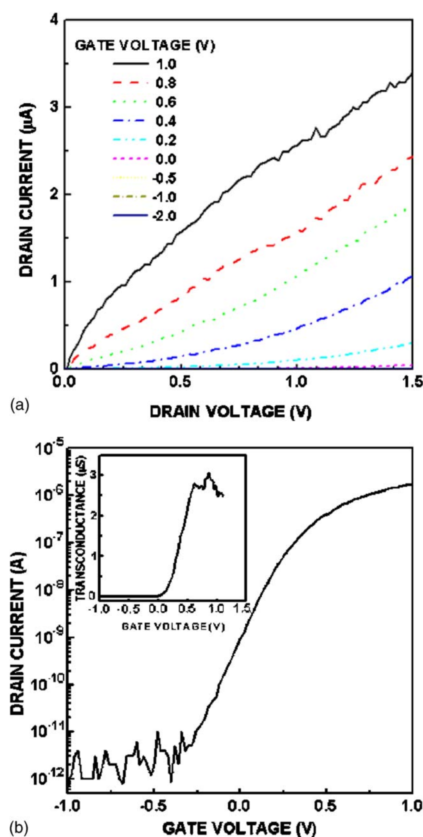

FIG. 2. (Color online) (a) Output characteristics of ZnO nanowire FET. The gate voltage range is from −2 to 1.0 V. (b) Transfer characteristic of the device with 0.8 V of source-drain voltage. Insert is transconductance curve of the device. The saturation value is 3.06 μS.

The field effect mobility (μ), of the ZnO nanowire FET, can be derived using the following relationship[18]

$$\mu = \frac{Lg_m}{WC_iV_{ds}},$$

where L, W, and C_i are the channel length, channel width, and the capacitance per unit channel area, respectively. C_i is calculated using three-dimensional finite element method simulation (COMSOL Multiphysics™).[19] The simulation was carried out on the FET structure and the space around it [Fig. 3(a)]. The capacitance (C) can be obtained from the simulated electrical field at specified voltages (the channel and gate are set to ground and 1 V, respectively). The value of the capacitance is 3.86×10^{-17} F. The capacitance includes the components due to the fringing field which may act on the extended length of the entire nanowire beyond the physical gate. It should be noted that the simulation results [Fig. 3(b)] clearly show that the electrical field distributed outside the physical gate cannot be simply ignored as it is found to have comparable magnitudes to that within the physical gate. Therefore, the entire suspended nanowire between source and drain electrode is considered to be the semiconducting channel, having a capacitance per unit area of 6.67×10^{-4} F/m^2 ($C_i=C/WL$). The field effect mobility using this capacitance and the measured average dimensions is estimated to be 928 cm^2/V s. This is a factor of 6 greater than the best value reported previously for a ZnO FET.[10] All fabricated devices had a field effect mobility in the range of 800–1080 cm^2/V s.

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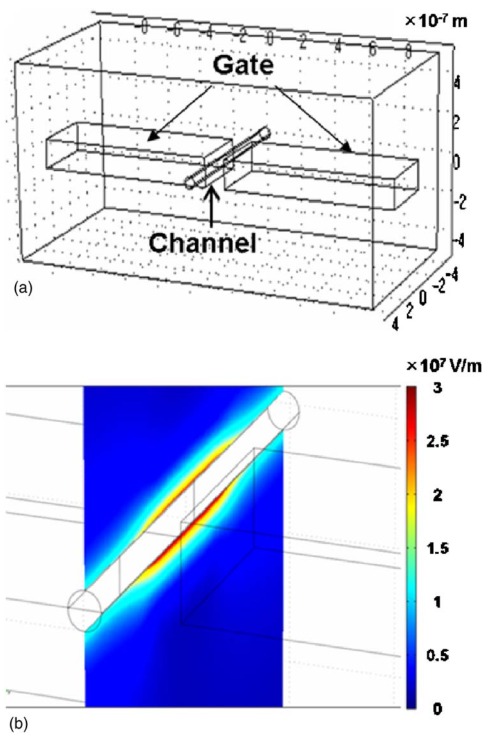

FIG. 3. (Color online) Simulation for the capacitance calculation of ZnO nanowire FET. (a) A domain for the capacitance simulation, which consists of the ZnO nanowire FET structure and the space around it. (b) Electrical field induced by a gate potential of 1 V.

To investigate the reliability of our devices, static gate bias stress measurements were carried out under a gate bias of 1 MV/cm over 20 000 s. Figure 4 shows the threshold voltage shifts plotted against bias stress time. The threshold voltage shift stabilizes after some initial drift and thereafter displays excellent stability. The threshold voltage increases from 0.4 to 0.84 V until the bias time reaches 1000 s and then it saturates. The metastability of threshold voltage has been extensively studied in *a*-Si:H thin film transistors (TFTs). In *a*-Si:H TFTs, the shift is due to charge trapping in the solid gate insulator at higher gate bias.[20] The dominant mechanism at low gate bias, on the other hand, is the creation of states or the breaking of bonds in the channel.[21] In

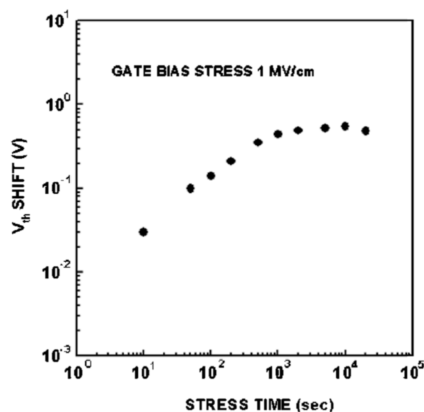

FIG. 4. Threshold voltage shift (difference between shifted threshold voltages and initial threshold voltage). The value is saturated after 1000 s.

the MASFET, the charge trapping in the gate insulator is insignificant since an air gap is used for the gate insulator. Therefore, by analogy with *a*-Si:H, creation of states or breaking of bonds in the ZnO nanowire may cause the threshold voltage shifts in the MASFET. The defects created in the channel, however, are possibly limited by the crystallinity and the physical dimensions of ZnO nanowire; hence the threshold voltage shift is saturated after a short time.

In summary, a FET structure using a suspended ZnO nanowire and self-aligned planar gate electrodes with air gap dielectric is demonstrated. The electrical characteristics show that ZnO nanowires can be comparable to CNTs in FETs,[15–17] especially as *n*-type FETs. Both *n*-type and *p*-type FETs are required for the replacement of Si complementary metal oxide semiconductor. Though there has recently been a report of a *n*-type CNT (Ref. 16) with better results than this ZnO MASFET, it is based on nonimplant chemical doping which is yet to be proven in terms of stability and reproducibility. With ZnO, the nanowires are always semiconducting. There is no issue about trying to control the metallic versus semiconducting properties as the case in CNTs. There is of course no ballistic transport in ZnO. However, this may not be a drawback for ZnO in that all it means is that a single CNT with 1.2–3 nm can be compatible with a 60 nm ZnO nanowire in terms of current. Therefore, technology which uses ZnO for the *n*-type FET and CNTs for the *p*-type FET may be the answer to replace Si channels in future integrated circuits.

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