Key Engineering Materials Vol. 443 (2010) pp 504-509
Online available since 2010/Jun/02 at www.scientific.net

doi:10.4028/www.scientific.net/KEM.443.504

Sputter-Deposited ZrO_2 Gate Dielectric on High Mobility Epitaxial-GaAs/Ge Channel Material for Advanced CMOS Applications

Goutam Kumar Dalapati[1,a], Avishek Kumar[2,b], Andrew See Weng Wong[1,c], Manippady Krishna Kumar[1,d], Ching Kean Chia[1,e], Ghim Wei Ho[3,f] and Dongzhi Chi[1,g]

[1]Institute of Materials Research and Engineering, A*STAR (Agency for Science, Technology and Research), 3 Research Link, Singapore 117602

[2]School of Electrical & Electronic Engineering, Nanyang Technological University; Nanyang Avenue; Singapore 639798

[3]Department of Electrical & Computer Engineering, National University of Singapore, Singapore 119260

[a]dalapatig@imre.a-star.edu.sg, [b]avishek.eee@gmail.com, [c]wonga@imre.a-star.edu.sg, [d]kumarm@imre.a-star.edu.sg, [e]ck-chia@imre.a-star.edu.sg, [f]elehgw@nus.edu.sg, [g]dz-chi@imre.a-star.edu.sg

Keywords: III-V semiconductor; epi-GaAs; high-k; GaAs-MOS capacitor; frequency dispersion

Abstract. Sputtered-deposited ZrO_2 gate dielectric on epitaxial-GaAs/Ge substrates have been studied for complementary-metal-oxide-semiconductor (CMOS) applications. The epitaxial-GaAs (epi-GaAs) on Ge susbstrates with AlGaAs interlayer was grown by metal-organic chemical vapor deposition at 650^{o}C. High resolution transmission electron microscopy ((HRTEM) shows that the epilayers are free from arsenic anti-phase defects (APD). From secondary ion mass spectrometry, it was confirmed that the Ge diffusion is completely blocked by the AlGaAs layer and no Ge atoms are able to penetrate into the GaAs layer. The macroscopic surface roughness of epitaxial GaAs is ~5.3nm, whereas over 200x200nm is 0.4 nm, which is comparable with bulk GaAs. Althogh, the epi-GaAs has nano-scale surface features; the conduction-AFM shows electrically homogeneous surface. The electrical and interfacial properties of MOS capacitors with sputtered deposited ZrO_2 dielectric on epitaxial-GaAs/Ge and bulk GaAs substrates were investigated. The frequency dispersion and hysteresis voltage for directly deposited ZrO_2 on epi-GaAs is higher compared with bulk p-GaAs, however, it is comparable with bulk n-GaAs. The interfacial and electrical properties of ZrO_2 on epi-GaAs have shown to exhibit better electrical characteristics after post deposition annealing (PDA) at 400^{o}C. The apparent doping profile of the epitaxial layer is unchanged with PDA temperatures, which suggest the less cross-diffusion of Ge, Ga, and As during device fabrication. The degradation of the gate oxide quality and interface properties are mainly due to the high surface roughness of epitaxial layer and also presence of elemental out diffusion of Ga and As.

Introduction

The demand for low-power, ultrahigh-speed applications have pushed the performance of Si-based complementary-metal-oxide-semiconductor (CMOS) devices to their scaling limit. Thus, there is a need for other device enhancing methods to drive CMOS technology beyond 22nm node. In recent years, research focus has swung towards finding alternative materials that can support future high performance applications. High-k dielectrics and III-V compound semiconductors are the most strategic options for future CMOS applications due to their superior electron transport properties. Amongst them, GaAs shows six times higher electron mobility over Si makes it an attractive channel material for advance CMOS devices [1]. However, such promising channel materials must be able to be integrated onto large scale Si or Ge wafers in order to be used for industrial applications [2]. The integration of epitaxial GaAs (epi-GaAs) on Ge substrate would thus become a basic prerequisite in future CMOS devices.

Despite their very similar lattice constants and thermal expansion coefficients, monolithic integration of GaAs and Ge remains challenging. Numerous technical issues need to be overcome in obtaining good quality GaAs epilayer on Ge, such as the polar-nonpolar nature, and distinct optimum growth temperature between GaAs and Ge. GaAs grown at its optimum temperature on Ge will result in high Ge contamination, such as auto-doping and formation of Ge-based complexes, as significant Ge atoms will diffuse into the GaAs epilayer during growth, hence increases the surface roughness of the epi-layer. The high surface roughness of epi-layer degrades the interface properties as well as bulk oxide properties. Therefore, it is necessary to passivate the epi-layer by using high quality gate dielectrics. On the other hand, growing GaAs at low temperature to prevent the out-diffusion of Ge atoms will be trade off with high arsenic-antisite defects (APD) in GaAs.

The chemical and physical vapor depositions of a dielectric on GaAs have already been shown to be effective in reduction of the interface state density and are therefore being considered as a viable alternative to passivate the GaAs surface [3-5]. Much progress has been made to form a high-quality gate dielectric on bulk-III–V semiconductor [3-6]. However, the integration of high-k dielectrics with epitaxial layer of GaAs on Ge (GaAs/Ge) is challenging due to lack of high quality epitaxial layer. The surface morphology of the epi-layer is very important for surface channel device. The bulk GaAs has surface roughness around ~0.3 nm, however, the epi-layer usually very rough and has nano-scale features. In this case, it is very important of surface passivation for epi-layer. In this work, a systematic and comprehensive study is presented on the integrity of high-k gate dielectric on epitaxial GaAs/Ge substrates. The results are compared with bulk p-type and n-type GaAs substrates. Thin films of zirconium oxide (ZrO_2) high-k material with TaN metal gate is evaluated on epitaxial-GaAs/Ge substrates and both n- and p-type bulk GaAs substrates. Electrical characteristics and physical analysis have also been done to understand the impact of the material and processing conditions for high-quality gate stack on epitaxial GaAs/Ge structure.

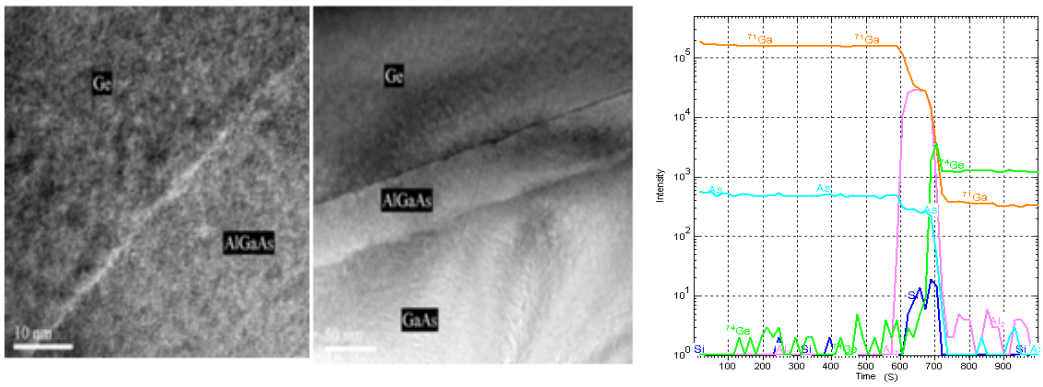
Experimental

Metal-oxide-semiconductor capacitors were fabricated on epi-GaAs substrates. The epi-GaAs layers were grown at 650°C by using metal organic chemical vapor deposition method on Ge substrates. Vicinal Ge (100) substrates with 6° offcut toward the (111) plane were used to ensure that the GaAs epilayer grown on Ge is free from APD defects. The thin films of $Al_{0.95}Ga_{0.05}As$ layer were grown on Ge substrates to reduce the out-diffusion of Ge into epi-GaAs layer. Prior to the growth of $Al_{0.95}Ga_{0.05}As$ and GaAs layers, Ge substrate was heated up to and kept at 650°C for 5 min to remove the native oxide layer under H_2 environment in the absence of As. Tertiarybutylarsine and trimethylaluminum (TMAl) were introduced into the reactor for the growth of AlGaAs interfacial layer. Finally, by switching TMAl to trimethylgallium (TMGa), a 500 nm GaAs epilayer was grown at 0.32 nm/s. Prior to the oxide deposition, the wafers were degreased using isopropanol, cleaned in HF solution (1%) for 3 mins to remove native oxide. The ZrO_2 dielectric layers were deposited at room temperature by sputter using ZrO_2 target and 60 W rf power in an Ar ambient at 3 mTorr working pressure. Post-deposition annealing (PDA) was carried out in N_2 ambient at 300-600°C for 1 min by rapid thermal annealing. TaN metal, deposited by sputtering, was used as the gate electrode (area: $7.8x10^{-3}$ cm^2). Low resistance ohmic back contact is formed by depositing Ti/Pt/Au alloy on p-GaAs substrate, Au- GeNi alloy on n-GaAs substrate and Au on Ge substrate.

Results and Discussion

The quality of the epi-GaAs was investigated by using high-resolution transmission electron microscopy (HRTEM), secondary ion mass spectrometry (SIMS), and atomic force microscopy (AFM). Fig. 1 depicts the HRTEM images and secondary ion mass spectrometry profiles of the GaAs/AlGaAs/Ge samples. The AlGaAs thickness is 50nm as determined from TEM image. It is observed that a smooth and abrupt interface exists between GaAs, AlGaAs and Ge, indicating good quality epi-layer and the epi-layers are free from APD defects as shown in Fig. 1(a). The corresponding secondary ion mass spectrometry profiles are shown in Fig. 1(b). It was found that

the Ge diffusion is completely blocked by the AlGaAs layer and no Ge atoms are able to penetrate into the GaAs layer as shown in Fig. 1(b), attributed to the higher Al–As bonding energy [7].



(a) (b)

Fig. 1 (a) HR-TEM and (b) SIMS profiles of GaAs/Ge structure.

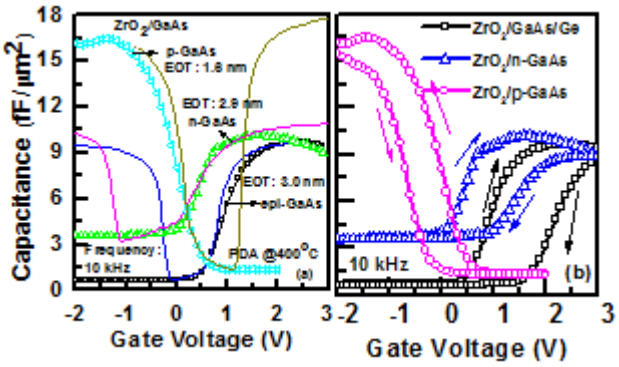


Fig. 2 (a) C–V characteristics of GaAs MOS capacitor at 10 kHz. ZrO_2 (10nm) gate dielectric deposited on epi-GaAs and bulk-GaAs. (b) Hysteresis characteristics for the same gate stacks.

Fig. 2 shows the capacitance-voltage (C-V) characteristics of sputtered ZrO_2 on bulk p-GaAs, bulk n-GaAs, and epi-GaAs after PDA at 400°C. It is observed that ZrO_2 on bulk p-GaAs showed better C-V characteristics as compared to ZrO_2 on n-GaAs and epi-GaAs. The C-V curves show clear existence of accumulation and depletion regimes for the sample annealed at 400°C. It is evident from Fig. 2 that ZrO_2/p-GaAs shows a higher maximum accumulation capacitance (C_{ox}) of (16.5 fF/μm^2), as compared to ZrO_2/n-GaAs and ZrO_2/epi-GaAs gate stacks. Even though the physical thckness of ZrO_2 is ~10nm, as measured from TEM, the large difference in C_{ox} obtained for p-GaAs and n-GaAs-based devices implies that p-GaAs and n-GaAs have different interfacial properties. It is also observed that epi-GaAs and bulk n-GaAs have similar interfacial properties, as the C_{ox} for ZrO_2 on bulk n-GaAs and epi-GaAs is comparable with each other (10.2fF/μm^2 and 9.7fF/μm^2, respectively). The equivalent oxide thickness (EOT) was extracted by fitting the C-V curves at 10 kHz in Fig. 2(a) and with the simulated C-V curve that accounts for quantum mechanical effects. The values are 1.6nm, 2.9nm, and 3.0nm for ZrO_2/p-GaAs, ZrO_2/n-GaAs, and ZrO_2/epi-GaA, respectively. The V_{FB} for ZrO_2/p-GaAs, ZrO_2/n-GaAs, and ZrO_2/epi-GaAs are 0.1V, 0.6V and 0.8V, respectively. The fixed oxide charge (Q_f/q) was found to be -9.7 x 10^{12}cm^{-2}, -9.6 x 10^{12}cm^{-2}, and -9.7 x 10^{12}cm^{-2} for ZrO_2/p-GaAs, ZrO_2/n-GaAs, and ZrO_2/epi-GaAs, respectively.

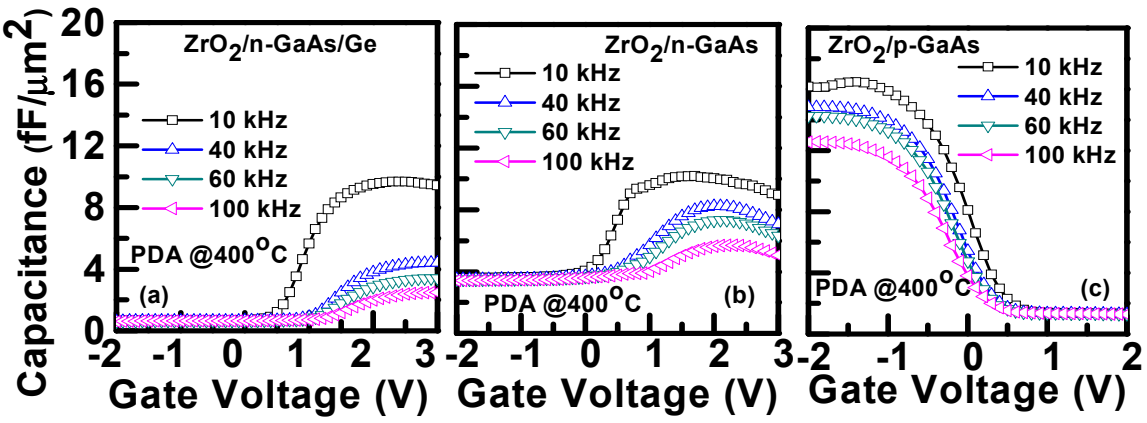


Fig. 3 Frequency dispersion in C-V characteristics between 10 kHz and 100 kHz for ZrO_2 deposited on (a) epi-GaAs, (b) n-GaAs, and (c) p-GaAs, respectively and annealed at 400°C.

The C-V curves measured at different frequencies shows the frequency dispersions in accumulation and depletion regions, as shown in Figs. 3(a), (b), and (c). The amounts of frequency dispersions in accumulation capacitance per decade, evaluated as (ΔC_{ox}) is ~57% for the ZrO_2/epi-GaAs gate stack. The values are 44% and 25% for ZrO_2 on n-GaAs and p-GaAs, respectively. The frequency dispersion for ZrO_2/n-GaAs gate stack, which is higher compared with ZrO_2/p-GaAs gate stack is due to the difference in electron and hole trap time constants in the n-type and p-type GaAs substrates [8]. This time constant vary with differences in the conduction and valence band densities of states, capture cross sections of electron versus holes, and any energetic asymmetries in the D_{it} distribution. Although, the epi-GaAs is n-type, the frequency dispersion even higher compared with n-GaAs, which may be due to high surface roughness of epi-GaAs. The surface roughness of epi-GaAs and bulk-GaAs were measured by using atomic force microscope (AFM). The RMS surface roughness is 5.3nm for epi-GaAs layer on a scale bar of 2μm and it is 0.4nm over 200 x 200nm. However, the RMS surface roughness for bulk p-GaAs is 0.3nm on a scale bar of 2μm. Although, the epi-GaAs has high surface roughness, the value (5.3nm) is comparable and even lower compared with the reported results [9]. Careful simultaneous observations of the topographic profile in comparison with the current profile using conduction-AFM (C-AFM) reveal that the current mapping reflect electrically homogeneous surface topography of epi-GaAs.

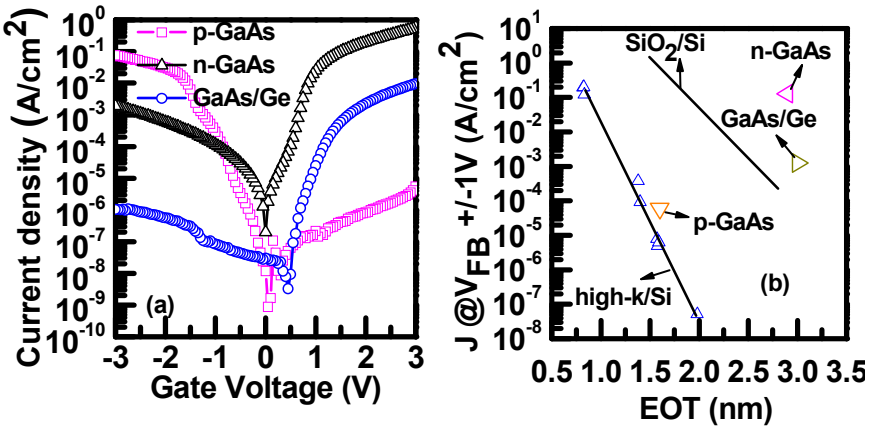


Fig. 4 (a) J-V Characteristics (b) Jg at V_{FB}+/-1 versus EOT of ZrO_2 on epi-GaAs and bulk-GaAs.

Leakage current measurements have been performed for further investigation of the quality of the ZrO_2/GaAs gate stack. Fig. 4(a) shows the current density-voltage (J-V) characteristics of the GaAs MOS capacitor. The current density of the GaAs MOS structure is ~10^{-3} A.cm^{-2} @ V_{FB}+1 V for directly deposited ZrO_2 gate dielectric on epi-GaAs. Fig. 4(b) shows the gate leakage current

density at V_{FB} +/-1 V against EOT. The result shows that, even though PVD ZrO_2 on n-GaAs is leakier than high-k on Si, ZrO_2/p-GaAs can achieve a lower leakage current than SiO_2 on Si for the same EOT.

Since our eventual interest of ZrO_2 on epi-GaAs, we did further investigation on TaN/ZrO_2/epi-GaAs gate stack, focusing on the effect of thermal process after sputter. A cross-sectional HRTEM images of TaN/ZrO_2/epi-GaAs gate stack after PDA at (a) 400°C and (b) 500°C are shown in Fig. 5. The physical thickness of ZrO_2 is 10nm. A smooth and thin interface layer between ZrO_2 and epi-GaAs layers is observed after PDA at 400°C. However, the rough and thick interfacial layer observed after PDA at 500°C, as shown in Fig. 5.

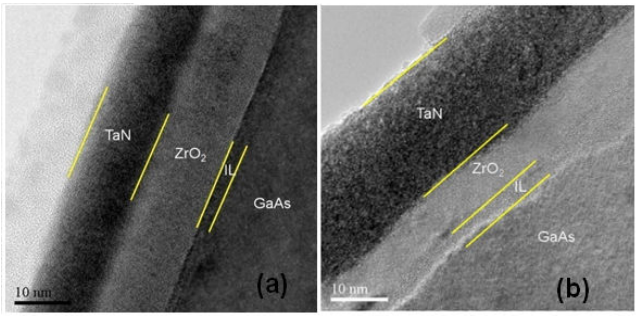


Fig. 5 HRTEM images of TaN/ZrO_2/epi-GaAs gate structure with PDA at (a) 400°C and (b) 500°C.

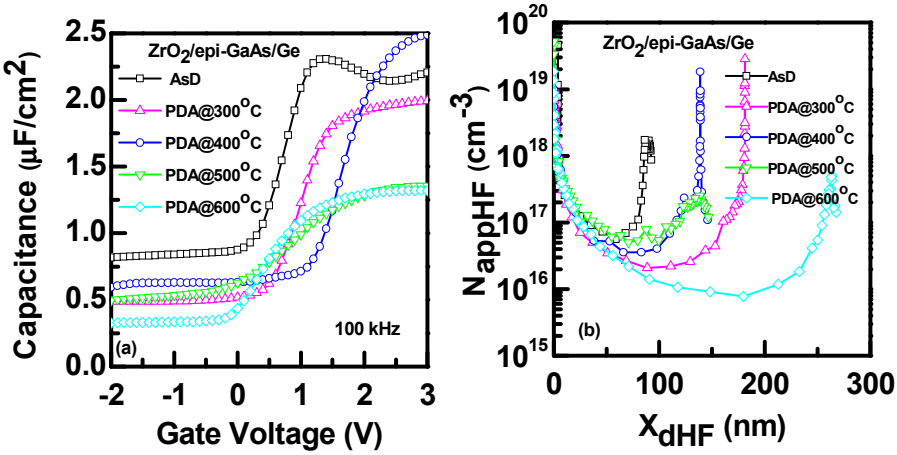


Fig. 6 (a) C–V characteristics for various PDA temperatures for 10nm thick ZrO_2 on epi-GaAs. (b) Apparent doping profiles for the epi-GaAs obtained from MOS high frequency C–V characteristics.

Fig. 6(a) shows the C–V characteristics of TaN/ZrO_2/epi-GaAs MOS structure for different PDA temperatures of 300°C, 400°C, 500°C, and 600°C, measured at a frequency of 100 kHz. The C–V characteristics show that the stretch-out effect of the C–V curves, which is associated with the interface-state densities, depends on the PDA temperature. The sample annealed at 400°C exhibits minimum stretch-out effect and maximum accumulation capacitance. However, the streched-out effect increased for the sample annealed after 500°C, most likely due to the degradation of the interface layer at high temperature. It is worth noting that the sample annealed at 500°C exhibits a decrease in accumulation capacitance, which suggests the formation of thick interfacial layer. It is also observed that bulk n-GaAs and epi-GaAs showed small variations in V_{FB} with different PDA temperatures. Hence, thermal stability of V_{FB} for epi-GaAs is comparable to bulk n-GaAs. The apparent susbtrates doping concentration was extracted from the C-V curves measured at 100 kHz. The depletion depth (X_{dHF}) and apparent doping (N_{appHF}) of GaAs as a function of applied gate potential (V_G) are obtained as [10]:

$$X_{dHF}(V_G) = \varepsilon_{GaAs}\left(\frac{1}{C_{HF}(V_G)} - \frac{1}{C_{OX}}\right) \quad \text{and} \qquad (1)$$

$$\frac{1}{N_{appHF}(V_G)} = \left(\frac{q\varepsilon_{GaAs}}{2}\right)\left(\frac{\delta(1/C_{HF}^2(V_G))}{\delta V_G}\right) \quad (2)$$

where, ε_{GaAs} is the permittivity of GaAs, C_{HF} is the high-frequency capacitance, C_{ox} is the maximum accumulation capacitance per unit area, and q, the electronic charge. Fig. 6(b) shows the variation of apparent doping profiles with depletion depth for different PDA temperatures. From the Fig 6(b), it is observed that the apparent substrates doping varying from ~$8x10^{16}cm^{-3}$ fo as deposited sample to $10^{16}cm^{-3}$ for sample annealed at 600°C. Although, there is no significance out-diffusion of Ge across the GaAs/Ge heterostucture, the apparent substrates doping slightly decreases with PDA tempertures, which may be due to cross-diffusion at the hetero-interface, however, the exact meachanism is not clear at the moment.

Summary

The feasibility of integration of epitaxial-GaAs on Ge substrates and ZrO_2 gate dielectric is demonstrated in this study. The MOCVD grown epitaxila-GaAs shows high quality epi-layer on Ge substrates for III-V CMOS application in Si platform. Presence of thin AlGaAs layer between GaAs and Ge substrates significantly reduced the Ge out-diffusion across GaAs/Ge hetero-interface. The epi-GaAs MOS device characteristics such as frequency dispersion, hysteresis voltage, and leakage current density comparable with bulk-n-GaAs. The optimum PDA condition on ZrO_2 on epi-GaAs is found to be 400°C. High-resolution TEM images show the thick interfacial layer for sputtered ZrO_2 on epi-GaAs after annealed at 500°C. The apparent substrate doping varying slightly with PDA temperatures. The results demonstrate a good feasibility for epi-GaAs with sputtered ZrO_2 dielectric for advanced III-V based CMOS application in Si platform.

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Advances in Materials Processing IX
doi:10.4028/www.scientific.net/KEM.443

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